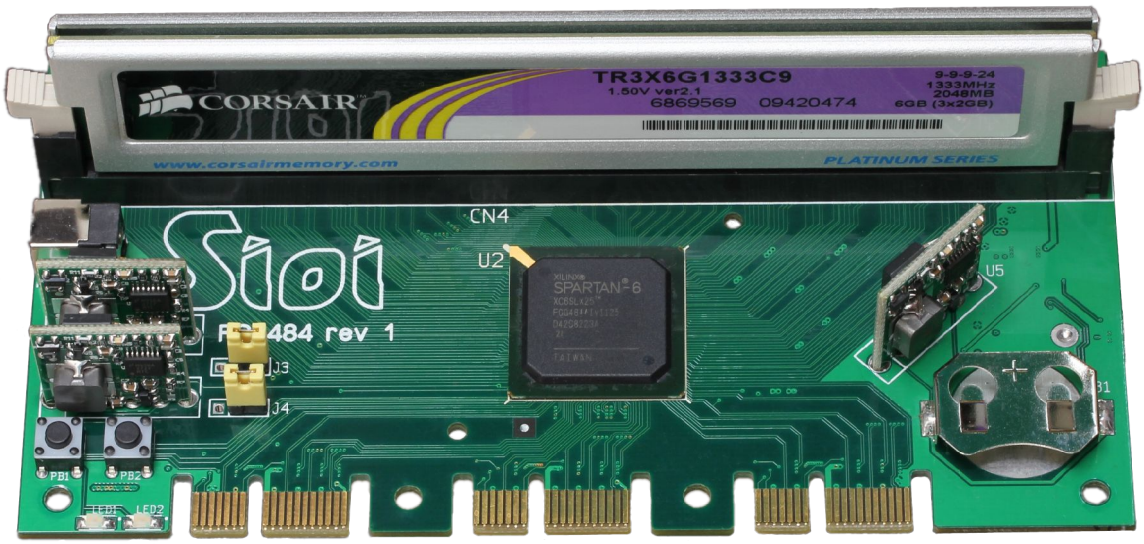
Xilinx Spartan 6 + DDR3 DIMM development boards



Introduction

The SiOI FS6484 are a family of Xilinx Spartan 6 FPGA development boards with support for FPGAs of medium to large size, up to 8GB of DRAM and six versatile expansion ports.

Applications

- Student lab demonstrator board
- High speed data capture
- High speed data output
- Flexible data buffering – up to 8GB @ up to 2.4 GBPS

Physical

- Dimensions 143mm x 74mm x ~44mm
- Weight
  - 68g FS6484 main board
  - 105g with typical DIMM
  - ~300g with DIMM and AC-DC converter
  - ~400g packaged shipping weight
- Power consumption
  - 475mA from 9V input typical for LX25 with 2GB DIMM
  - 510mA from 9V input typical for LX75 with 2GB DIMM
  - 1.15A from 9V input typical for LX150 with 2GB DIMM

Key components

The key components of the FS6484 are:

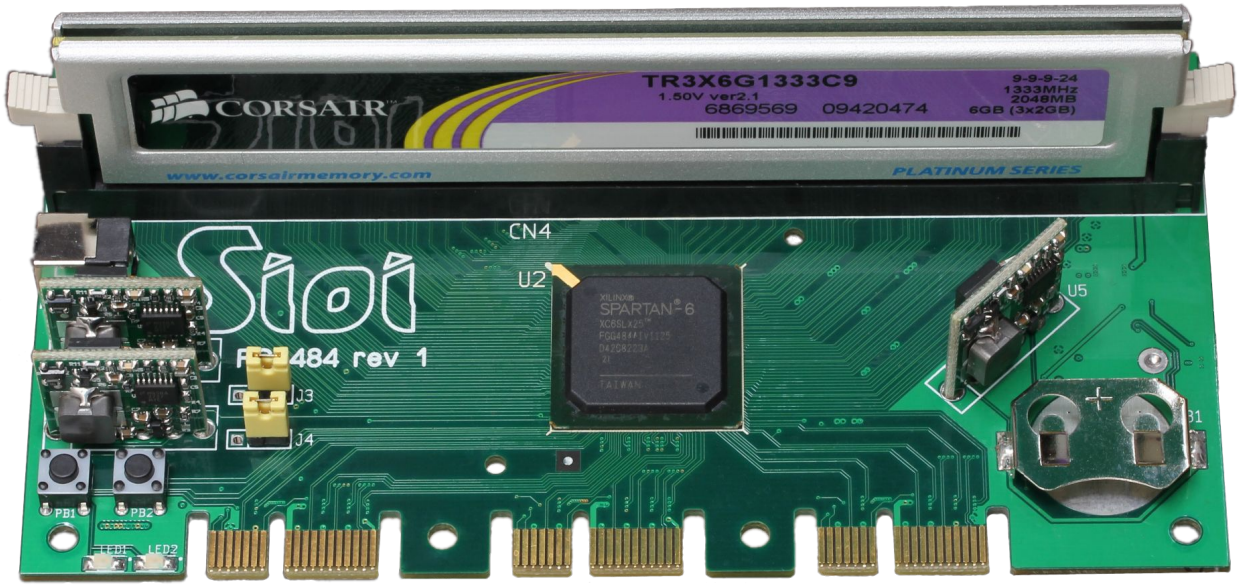
- Xilinx Spartan 6 LX FPGA
  - LX25 / LX75 / LX100 / LX150 fully supported
  - LX45 partially supported: two of the six expander ports drop from 16 FPGA IO pins down to 14 FPGA IO pins with this chip
  - FPGA speed grades –3, –3N, –2 supported
  - Commercial and Industrial temperature grades supported
  - FPGA speed grade -1L supported by design, email for availability
- DDR3 UDIMM 240 pin non-ECC 1.5V 1GB / 2GB / 4GB / 8GB DRAM
- NXP LPC1111 50MHz Cortex M0 microcontroller
- Crystal oscillator, 62.5 MHz low jitter
- Xilinx standard 14 pin JTAG header
- Two user controlled LEDs
- Two user defined push buttons
- CR2032 battery slot

Kit contents

FS6484 purchases includes these items:

- FS6484 main board
- Power supply AC 100V-240V in, DC 9V out. 4A for LX100 and LX150 boards, 2A for others
- DDR3 UDIMM 8GB / 4GB / 2GB / 1GB / or no DIMM at all depending on your choice at time of purchase
- DRAM controller Verilog IP core DDR3 DIMM 604 MT/sec, if chosen at time of purchase
- Reference design: MicroBlaze MCS + DRAM + UART + GPIO, if your purchase includes the DRAM controller IP core
- Manual and Schematic

Here's what you get:



Brand of DIMM may vary from that shown
Size of DIMM is a purchase time option
Purchase without a DIMM is also an option

9V DC power supply.
Plug OD 5.5mm ID 2.5mm
inner +ve outer -ve

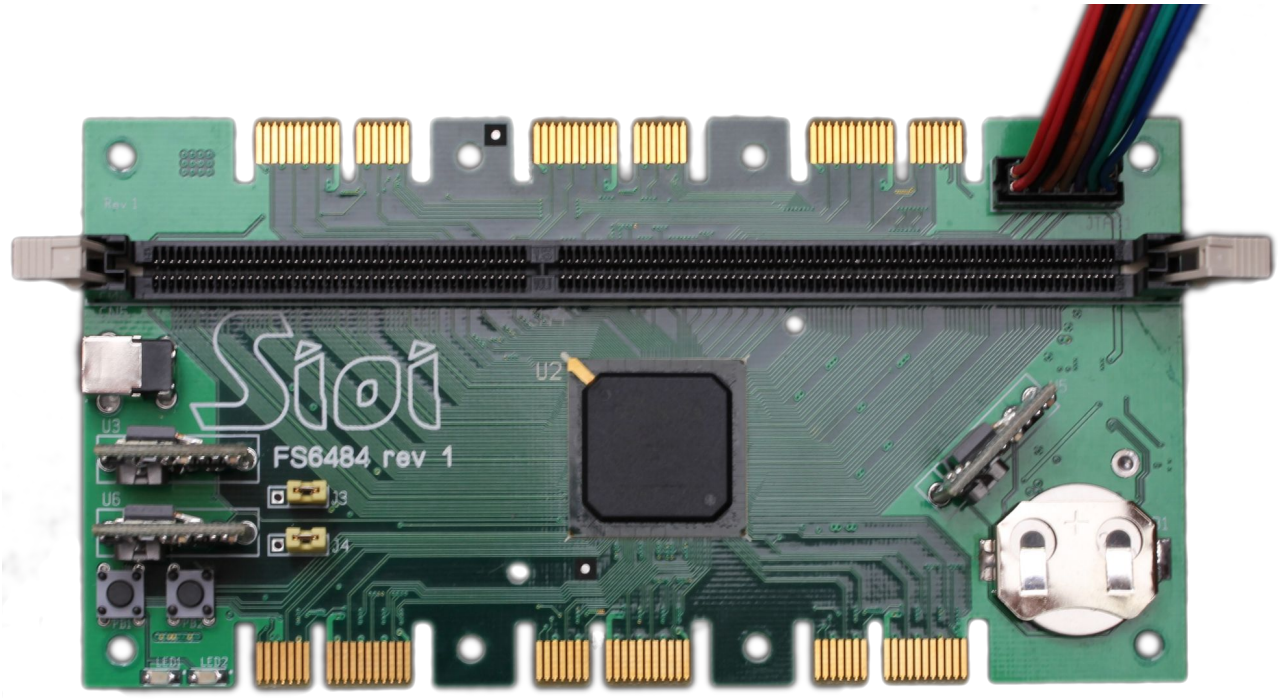
Attaching the power regulator

- Please attach the AC-DC power adapter like this:

- The AC-DC adapter provides the FS6484 with a supply of DC power with the following specifications:
  - DC 9V ±20%
  - Maximum current 2A (LX25 and LX75)
  - Maximum current 4A (LX100 and LX150)
  - Plug OD 5.5mm ID 2.5mm, inner +ve and outer -ve
- To reset the FPGA you can disconnect the power and then reconnect it. The FS6484 has built in circuitry to correctly reset the FPGA on power up.
- The FPGA is automatically reset when programming the FPGA through the JTAG port.

Attaching a JTAG programmer

- To program the FPGA please connect a JTAG programmer like this:



- Use a JTAG cable that matches the Xilinx standard 14 pin 2mm pitch JTAG header
- The SIOI parallel port JTAG cable or the Xilinx USB cable work well.

Inserting the battery (LX75 / LX100 / LX150 only)

The larger FPGAs support battery backed SRAM retention of AES keys for encrypted bitstream security. The FS6484 provides a battery holder for a CR2032 lithium battery for this purpose.

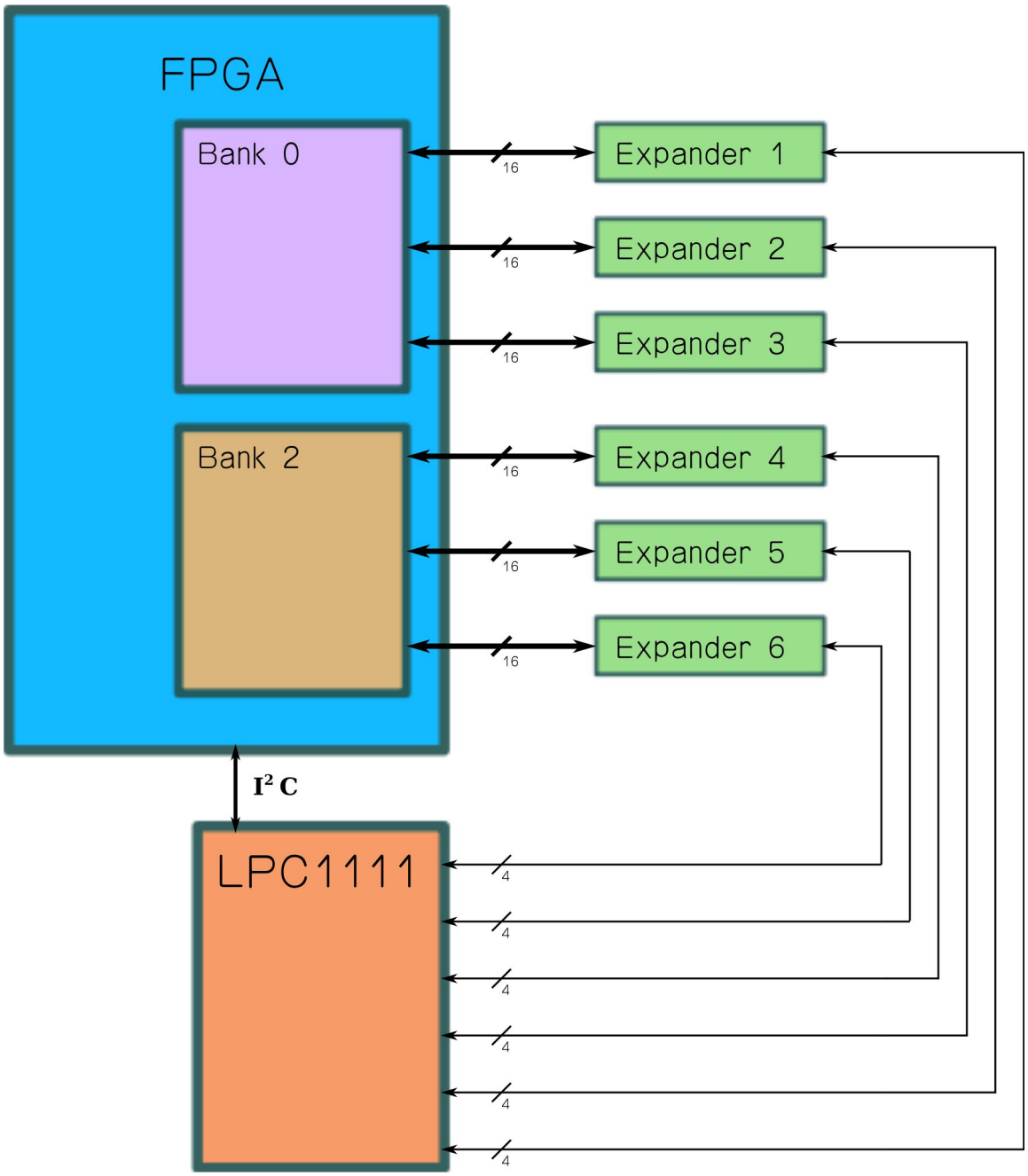
Take care not to insert the battery upside down – that could damage the FPGA!

Insert the battery from the front of the board, with the positive side facing up:

Insert the coin until it reaches the back of the battery holder:

Expansion connectors

The six expansion ports connect to FPGA bank 0 and bank 2 and also to the LPC1111 microcontroller, as shown below:



Each of the six expansion ports has the following features:

- 16 signal lines from the FPGA
- 4 signal lines from the microcontroller
- DC 9V ±20% power, available at one pin
- FPGA VCCO power at two pins
- The open drain Global Reset signal, available at one pin (allows reset in and reset out)

Expander FPGA signals

The 16 signal lines from the FPGA have these characteristics:

- Routed as 8 differential pairs
- Each differential pair can be used as such or alternatively can be configured as two single ended signals
- FPGA signals are routed with 50 ohm single ended characteristic impedance and 100 ohm differential characteristic impedance
- The first signal pair are GCLK signals that can be used to input clock signals to the FPGA
- One of the signals in the second pair is a VREF signal that can be re-purposed as a voltage reference input when using signaling standards such as HSTL or SSTL
- Carefully designed expansion cards should be able to achieve data transfer rates up to the limits of the Spartan 6 FPGA:
  - 1080 Mbps for –3 speed grade FPGAs
  - 1050 Mbps for –3N speed grade FPGAs
  - 950 Mbps for –2 speed grade FPGAs
  - 500 Mbps for –1L speed grade FPGAs
  - Consult table 25 in Xilinx Data Sheet DS162 for more details
- Connected to FPGA bank 0 or FPGA bank 2

Spartan 6 bank 0 and bank 2 pins support a wide variety of signaling standards:

- LVTTL
- LVCMOS
- LVDS
- SSTL3
- SSTL2
- SSTL18_I
- HSTL_I
- HSTL_III
- HSTL_I_18
- HSTL_III_18
- TMDS
- others, see Xilinx SelectIO User Guide UG381 for details

Expander physical characteristics

- The edge connector used is the same as that used for PCIE x1. It features a 1mm pitch and has 36 connections configured as a group of 22 and a group of 14 with a keying spacer between the two groups

  Important: Do not insert the FS6484 into an actual PCIE slot! The connector is the same size but the voltages used are completely different and damage to the FS6484 would result.

- A suitable edge connector is FCI family 10018784 or similar
- Sullins part NWE18DHR is a straddle mount type edge connector that can be used for applications where the daughter card needs to sit in the same plane as the FS6484 main board
- An expansion board template for gEDA PCB CAD package available as a free download from the SiOI website

- The edge connector maintains characteristic impedance across board to board boundary and is rated for operation up to 5Gbps per signal pair, well above the top speeds achievable with a Spartan 6LX FPGA.

Expander board power

- The FPGA IO pins are powered from Bank 0 VCCO (CN1, CN2, CN3) or Bank 2 VCCO (CN6, CN7, CN8)
- Bank 0 VCCO can be powered from the on-board 3V2 supply or alternatively it can be externally user powered if jumper JP3 is opened up
- Bank 2 VCCO can be powered from the on-board 3V2 supply or alternatively it can be externally user powered if jumper JP4 is opened up
- VCCO power is connected at expander pin 23
- DC 9V ±20% power is available at expander pins 21 and 22

Expander microcontroller signals

Each expander port has 4 signal lines from the microcontroller, with these characteristics:

- 3.2V LVCMOS signaling
- software controllable as input, output or bidirectional
- suitable for low speed housekeeping tasks such as I^2C device identity interrogation or control register setting.

The LPC1111 microcontroller can be programmed with user firmware through its SerialWire Debug (SWD) port. The SWD port signals are available on expander CN2 pins 34 and 35.

LPC1111 user firmware can be written in the low cost LPCxpresso IDE:

http://ics.nxp.com/lpcxpresso/

Compiled LPC1111 firmware can be downloaded into the LPC1111 using a low cost USB to SerialWire adapter such as NXP LPCxpresso part OM11049,598 (US$26.25 from DigiKey)

Expander port signal assignments

The connections for the expansion ports are shown on the following pages.

Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
0	TR	IO_L36P_GCLK15_0	IOCP	CN1-4	D11		GCLK
0	TR	IO_L36N_GCLK14_0	IOCM	CN1-6	C12		GCLK
0	TL	IO_L1P_HSWAPEN_0	IOVP	CN1-10	A3		
0	TL	IO_L1N_VREF_0	IOVM	CN1-12	A4		Vref
0	TL	IO_L32P_0	IO2P	CN1-16	D7		
0	TL	IO_L32N_0	IO2M	CN1-18	D8		
0	TL	IO_L6P_0	IO3P	CN1-28	B8		
0	TL	IO_L6N_0	IO3M	CN1-30	A8		
0	TL	IO_L3P_0	IO4P	CN1-3	D6		
0	TL	IO_L3N_0	IO4M	CN1-5	C6		
0	TL	IO_L2P_0	IO5P	CN1-9	C5		
0	TL	IO_L2N_0	IO5M	CN1-11	A5		
0	TL	IO_L4P_0	IO6P	CN1-15	B6		
0	TL	IO_L4N_0	IO6M	CN1-17	A6		
0	TL	IO_L5P_0	IO7P	CN1-27	C7		
0	TL	IO_L5N_0	IO7M	CN1-29	A7		
			GP0	CN1-34		13	
			GP1	CN1-36		17	
			GP2	CN1-33		12	
			GP3	CN1-35		14	

Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
0	TL	IO_L34P_GCLK19_0	IOCP	CN2-4	B10		GCLK
0	TL	IO_L34N_GCLK18_0	IOCM	CN2-6	A10		GCLK
0	TL	IO_L8P_0	IOVP	CN2-10	C9		
0	TL	IO_L8N_VREF_0	IOVM	CN2-12	A9		Vref
0	TR	IO_L50P_0	IO2P	CN2-16	B14		
0	TR	IO_L50N_0	IO2M	CN2-18	A14		
0	TR	IO_L47P_0	IO3P	CN2-28	E14		LX45 NC
0	TR	IO_L47N_0	IO3M	CN2-30	F15		LX45 NC
0	TL	IO_L7P_0	IO4P	CN2-3	D9		
0	TL	IO_L7N_0	IO4M	CN2-5	C8		
0	TL	IO_L33P_0	IO5P	CN2-9	D10		
0	TL	IO_L33N_0	IO5M	CN2-11	C10		
0	TL	IO_L35P_GCLK17_0	IO6P	CN2-15	C11		GCLK
0	TL	IO_L35N_GCLK16_0	IO6M	CN2-17	A11		GCLK
0	TR	IO_L49P_0	IO7P	CN2-27	D14		
0	TR	IO_L49N_0	IO7M	CN2-29	C14		
			GP0	CN2-34		19	SWCLK
			GP1	CN2-36		20	
			GP2	CN2-33		2	
			GP3	CN2-35		25	SWDIO

Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
0	TR	IO_L37P_GCLK13_0	IOCP	CN3-4	B12		GCLK
0	TR	IO_L37N_GCLK12_0	IOCM	CN3-6	A12		GCLK
0	TR	IO_L38P_0	IOVP	CN3-10	C13		
0	TR	IO_L38N_VREF_0	IOVM	CN3-12	A13		Vref
0	TR	IO_L65P_SCP3_0	IO2P	CN3-16	B18		
0	TR	IO_L65N_SCP2_0	IO2M	CN3-18	A18		
0	TR	IO_L46P_0	IO3P	CN3-28	H13		LX45 NC
0	TR	IO_L46N_0	IO3M	CN3-30	G13		LX45 NC
0	TR	IO_L51P_0	IO4P	CN3-3	C15		
0	TR	IO_L51N_0	IO4M	CN3-5	A15		
0	TR	IO_L63P_SCP7_0	IO5P	CN3-9	B16		
0	TR	IO_L63N_SCP6_0	IO5M	CN3-11	A16		
0	TR	IO_L66P_SCP1_0	IO6P	CN3-15	E16		
0	TR	IO_L66N_SCP0_0	IO6M	CN3-17	D17		
0	TR	IO_L64P_SCP5_0	IO7P	CN3-27	C17		
0	TR	IO_L64N_SCP4_0	IO7M	CN3-29	A17		
			GP0	CN3-34		21	
			GP1	CN3-36		23	
			GP2	CN3-33		22	
			GP3	CN3-35		24	

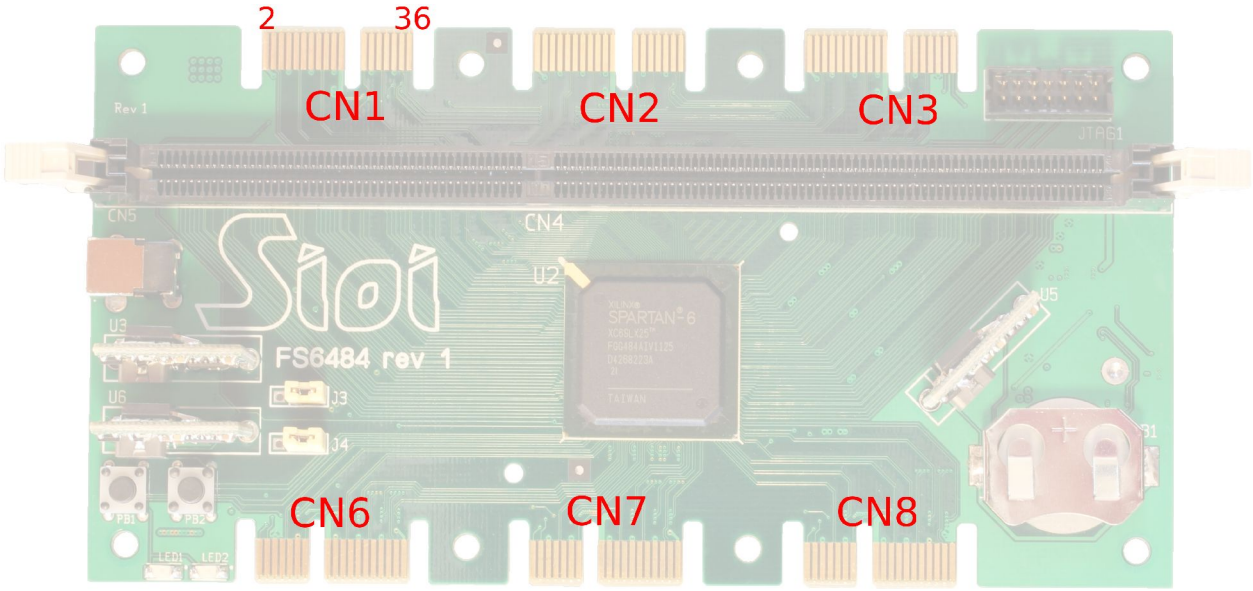
Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
2	BL	IO_L31P_GCLK31_D14_2	IOCP	CN6-4	AA12		GCLK
2	BL	IO_L31N_GCLK30_D15_2	IOCM	CN6-6	AB12		GCLK
2	BL	IO_L48P_D7_2	IOVP	CN6-10	Y7		
2	BL	IO_L48N_RDWR_B_VREF_2	IOVM	CN6-12	AB7		Vref
2	BL	IO_L49P_D3_2	IO2P	CN6-16	AA6		
2	BL	IO_L49N_D4_2	IO2M	CN6-18	AB6		
2	BL	IO_L57P_2	IO3P	CN6-28	AA4		
2	BL	IO_L57N_2	IO3M	CN6-30	AB4		
2	BL	IO_L43P_2	IO4P	CN6-3	Y9		
2	BL	IO_L43N_2	IO4M	CN6-5	AB9		
2	BL	IO_L45P_2	IO5P	CN6-9	AA8		
2	BL	IO_L45N_2	IO5M	CN6-11	AB8		
2	BR	IO_L12P_D1_MISO2_2	IO6P	CN6-15	U14		
2	BR	IO_L12N_D2_MISO3_2	IO6M	CN6-17	U13		
2	BL	IO_L62P_D5_2	IO7P	CN6-27	W4		
2	BL	IO_L62N_D6_2	IO7M	CN6-29	Y4		
			GP0	CN6-34		7	
			GP1	CN6-36		9	
			GP2	CN6-33		3	
			GP3	CN6-35		8	

Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
2	BR	IO_L30P_GCLK1_D13_2	IOCP	CN7-4	Y13		GCLK
2	BR	IO_L30N_GCLK0_USERCCLK_2	IOCM	CN7-6	AB13		GCLK
2	BL	IO_L41P_2	IOVP	CN7-10	AA10		
2	BL	IO_L41N_VREF_2	IOVM	CN7-12	AB10		Vref
2	BR	IO_L21P_2	IO2P	CN7-16	Y15		
2	BR	IO_L21N_2	IO2M	CN7-18	AB15		
2	BL	IO_L42P_2	IO3P	CN7-28	V11		
2	BL	IO_L42N_2	IO3M	CN7-30	W11		
2	BR	IO_L14P_D11_2	IO4P	CN7-3	AA18		
2	BR	IO_L14N_D12_2	IO4M	CN7-5	AB18		
2	BR	IO_L15P_2	IO5P	CN7-9	Y17		
2	BR	IO_L15N_2	IO5M	CN7-11	AB17		
2	BR	IO_L19P_2	IO6P	CN7-15	AA16		
2	BR	IO_L19N_2	IO6M	CN7-17	AB16		
2	BL	IO_L32P_GCLK29_2	IO7P	CN7-27	Y11		GCLK
2	BL	IO_L32N_GCLK28_2	IO7M	CN7-29	AB11		GCLK
			GP0	CN7-34		32	
			GP1	CN7-36		18	
			GP2	CN7-33		31	
			GP3	CN7-35		1	

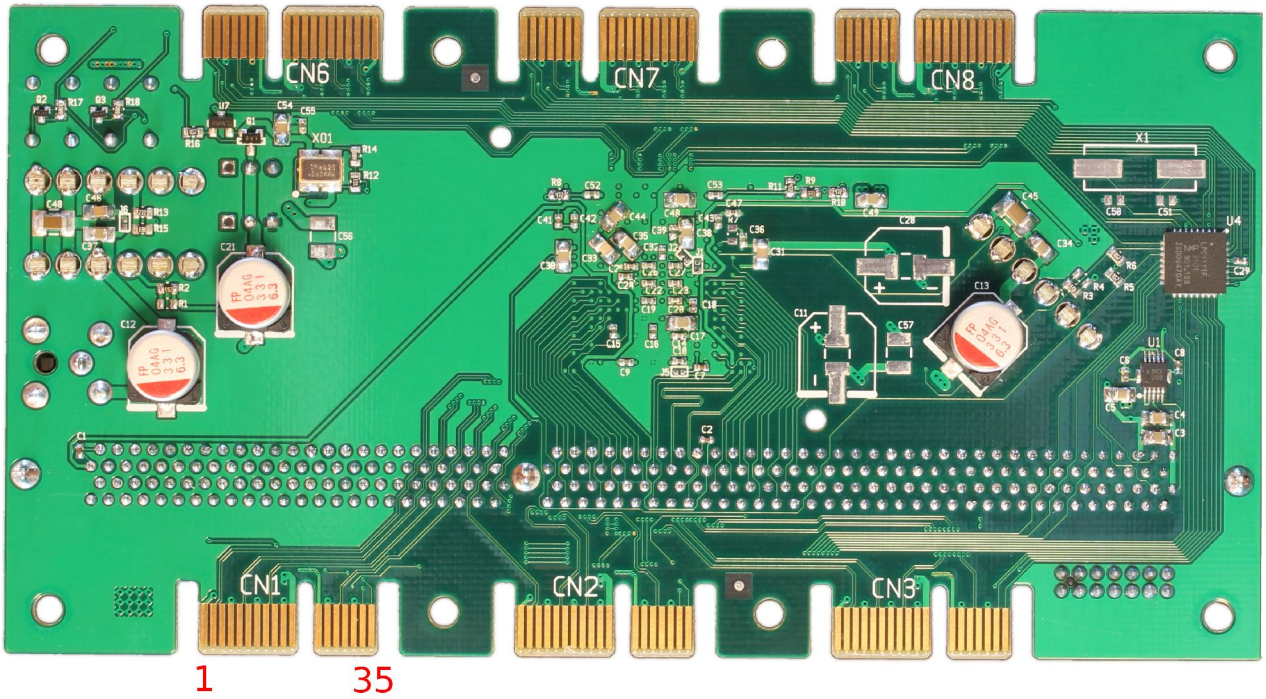
Bank	Corner	Pin Description	Name	Location	FPGA ball	CPU pin	Notes
2	BR	IO_L29P_GCLK3_2	IOCP	CN8-4	W12		GCLK
2	BR	IO_L29N_GCLK2_2	IOCM	CN8-6	Y12		GCLK
2	BR	IO_L16P_2	IOVP	CN8-10	AA14		
2	BR	IO_L16N_VREF_2	IOVM	CN8-12	AB14		Vref
2	BR	IO_L2P_CMPCLK_2	IO2P	CN8-16	AA21		
2	BR	IO_L2N_CMPMOSI_2	IO2M	CN8-18	AB21		
2	BR	IO_L5P_2	IO3P	CN8-28	Y19		
2	BR	IO_L5N_2	IO3M	CN8-30	AB19		
2	BR	IO_L13P_M1_2	IO4P	CN8-3	U15		M1 config mode select
2	BR	IO_L13N_D10_2	IO4M	CN8-5	V15		
2	BR	IO_L1P_CCLK_2	IO5P	CN8-9	Y21		SPI clk (from FPGA)
2	BR	IO_L1N_M0_CMPMISO_2	IO5M	CN8-11	AA22		M0 config mode select
2	BL	IO_L65P_INIT_B_2	IO6P	CN8-15	T6		
2	BL	IO_L65N_CSO_B_2	IO6M	CN8-17	T5		SPI CS# (from FPGA)
2	BR	IO_L3P_D0_DIN_MISO_MISO1_2	IO7P	CN8-27	AA20		SPI data, flash to FPGA
2	BR	IO_L3N_MOSI_CSI_B_MISO0_2	IO7M	CN8-29	AB20		SPI data, FPGA to flash
			GP0	CN8-34		27	
			GP1	CN8-36		30	
			GP2	CN8-33		26	
			GP3	CN8-35		28	

Connector orientation

The location of the six expansion connectors is shown below. The pin numbering orientation of the connectors is illustrated for CN1. CN1's leftmost pin on the topside is pin 2 while its rightmost pin on the topside is pin 36:



The rear side of the FS6484 is shown below. CN1's leftmost pin on the rear side is pin 1 while its rightmost pin on the rear side is pin 35:



Software Compatibility

The FS6484 is compatible with:

- LX25, LX45 and LX75: free Xilinx ISE WebPACK software
- LX100 and LX150: Xilinx ISE and EDK software
- All: free Xilinx MicroBlaze MCS soft CPU (free since version 13.4)
- All: free Xilinx SDK software (free since version 14.1)
- All: low cost NXP LPCXpresso IDE for LPC1111

FAQ

Q: 16 FPGA IOs is not enough for the expander I'm planning. What can I do ?

A: It is possible to combine two or three of the expander ports to provide 32 or 48 FPGA IOs plus 8 or 12 micro-contoller IOs. The expander ports are placed at 36.0mm intervals, so design your expander with a second 36 way edge connector located 36.0mm along from the first. Add a third 36 way edge connector located 72.0mm along from the first if required.

Please take care when using this approach – even small misalignment of multiple edge connectors can make it very difficult to physically plug the resulting expander into the FS6484. A good approach is to solder your edge connectors **last**, and get their location right by plugging everything together (including the FS6484) with a dry fit before soldering them to your expander PCB.

Q: I don't need the DDR3 DRAM but I do need more FPGA IOs. Can I re-purpose the DIMM slot as an extra expander port ?

A: Sure. The DIMM slot provides 120 signals from FPGA IO bank 1 and FPGA IO bank 3 as well as plenty of connections to the 1V5 power rail, the 750mV termination supply rail and the 750mV voltage reference. Two connections to the LPC1111 microcontroller are also provided.

Q: I plan to re-purpose the DIMM slot as an extra expander port, but I need 1.8V signaling. Is this possible ?

A: The voltage of the 1V5 power rail can be modified by changing the values of R1 and/or R2. The voltage is controlled by the equation:

$$V = \frac{600\text{mV} \times [10\text{K} + (R1 \| R2)]}{(R1 \| R2)}$$

The voltage may be modified in the range 0V9 to 3V2.
The 750mV termination rail and the 750mV voltage reference track 50% of the nominally 1V5 rail while it is in the range 1V5 to 2V5. Outside that range their behaviour is unspecified.
Please note that damage caused by incorrect circuit modifications to the FS6484 are not covered by the warranty.

Q: I was making some mods to my FS6484 and I accidentally applied +9V DC power to the bank 1 and bank 3 VCCO rails. The FPGA now seems to be dead, can you help me ?

A: Our warranty does not cover this situation, however we do provide an at-cost replacement service. Send us your dead FS6484 or provide proof that it has been destroyed (eg photo of it sawn in half) and we will sell you a replacement unit at cost price (the price of components plus assembly plus shipping). Please email us first for the current cost price and stock availability or lead time.

Q: The supplied IP core DRAM controller operates at 604 MT/s. Is it possible to push this up to higher rates ?

A: Yes. 604 MT/s was chosen as the easiest speed to work with based on the oscillator input of 62.5MHz and the DDR3 spec of 600MT/s minimum transfer speed. Operation at higher speeds such as 750 MT/s is certainly possible and operation at speeds of up to 1062.5 MT/s **may** be possible. Contact sales@sioi.com.au for further details.

Appendix A - Jumpers

The FS6484 has the following jumpers:

J1 - VFS
Type: Solder jumper SPST
Factory default: Open
Location: solder side, under FPGA
Purpose: Can be closed to connect VFS to the 3V2 rail. Close if required for fuse programming.

J2 - SUSPEND
Type: Solder jumper SPST
Factory default: Closed
Location: solder side, under FPGA
Purpose: Keeps SUSPEND input connected to GND to prevent FPGA from entering SUSPEND mode.

JP3 – Bank 0 VCCO power internal / external selection
Type: 100mil posts SPST
Factory default: Closed
Location: component side
Purpose: Powers bank 0 VCCO from the 3V2 rail (default). Open this jumper when powering bank 0 VCCO from an alternative external user supplied voltage.

JP4 – Bank 2 VCCO power internal / external selection
Type: 100mil posts SPST
Factory default: Closed
Location: component side
Purpose: Powers bank 2 VCCO from the 3V2 rail (default). Open this jumper when powering bank 2 VCCO from an alternative external user supplied voltage.

J5 – Bank 0 VREF supplementary
Type: Solder jumper SPST
Factory default: Open
Location: solder side, under FPGA
Purpose: Bank 0 has four VREF pins. When using VREF based signaling on Bank 0 all four of these pins should be tied to the VREF voltage. Three of the four Bank 0 VREF pins are connected to expanders CN1, CN2 and CN3 (one each) but the fourth bank 0 VREF pin is an orphan. To connect it up close J5, which connects it to the VREF pin on CN3. You should then ensure that the VREF pin on CN3 is driven to the appropriate voltage.

Contact information

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