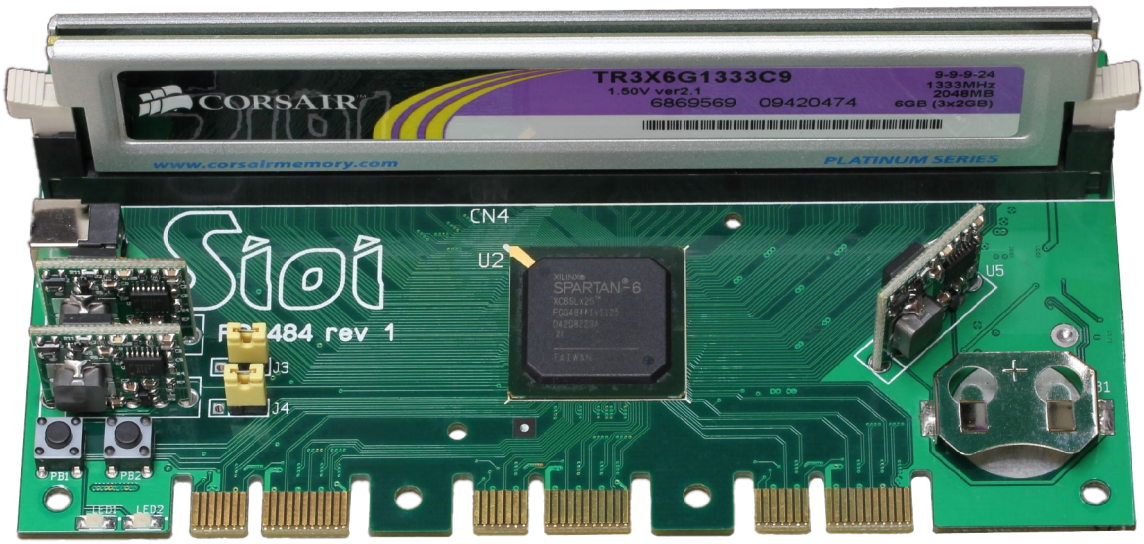
Xilinx Spartan 6 + DDR3 DIMM development boards



DESCRIPTION

The SiOI FS6484 are a family of Xilinx Spartan 6 FPGA development boards with support for FPGAs of medium to large size, up to 8GB of DRAM and six expansion ports.

- Spartan 6 LX25 / LX75 / LX100 / LX150 FPGA
- 1GB / 2GB / 4GB / 8GB DDR3 UDIMM (240 pin non-ECC)
- Peak DRAM bandwidth 4.8 GB/s
- NXP LPC1111 Cortex M0 microcontroller for low speed housekeeping tasks (I^2C and low speed SPI etc)
- Six expansion ports, each with 16 FPGA IO lines and 4 CPU IO lines
- Support for battery backed AES encryption keys (LX75 / LX100 / LX150 models only)
- 62.5MHz low jitter clock module
- JTAG port with standard Xilinx 14 pin header

APPLICATIONS

- Student lab demonstrator board
- High speed data capture
- High speed data output
- Flexible data buffering – up to 8GB @ up to 2.4 GBPS

PHYSICAL

- Dimensions 143mm x 74mm x ~44mm
- Weight
  - 68g FS6484 main board
  - 105g with typical DIMM
  - ~300g with DIMM and ACDC converter
  - ~400g packaged shipping weight
- Power consumption
  - 475mA from 9V input typical for LX25 with 2GB DIMM
  - 510mA from 9V input typical for LX75 with 2GB DIMM
  - 1.15A from 9V input typical for LX150 with 2GB DIMM

KEY COMPONENTS

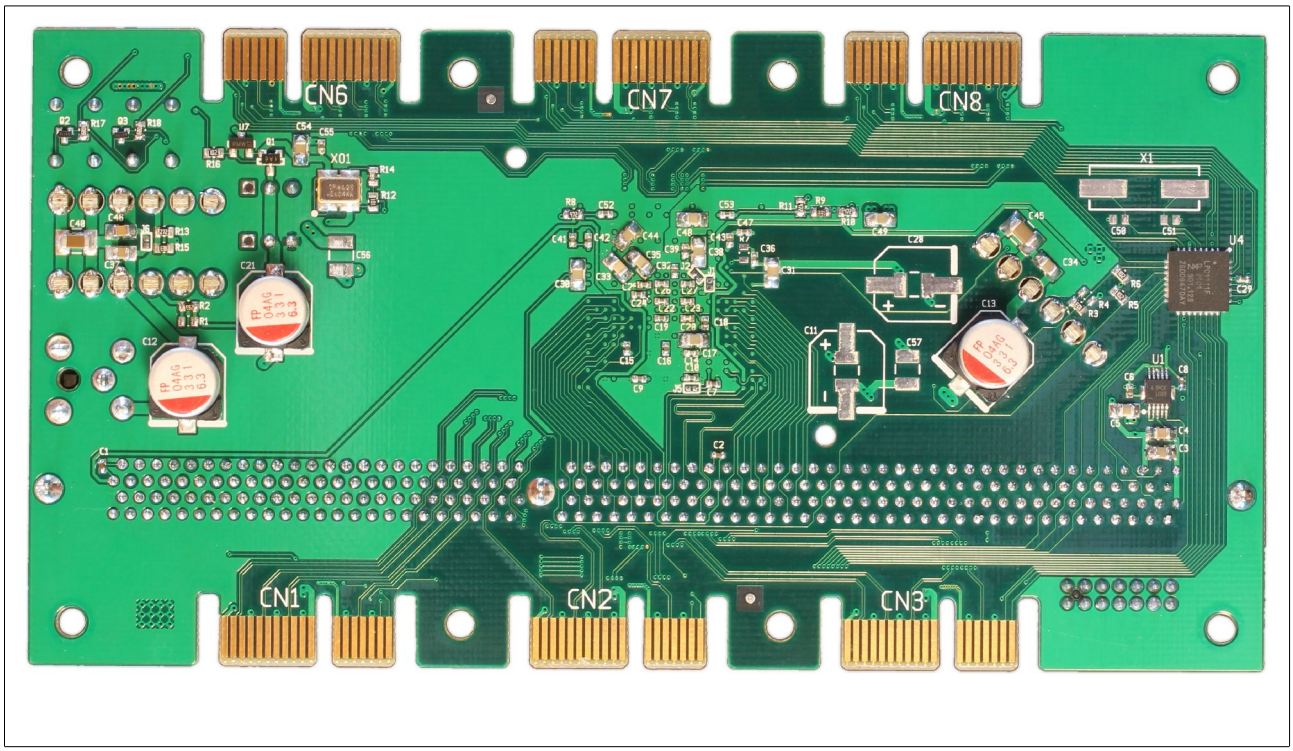
- Xilinx Spartan 6 LX FPGA
- LX25 / LX75 / LX100 / LX150 fully supported

- LX45 supported but two of the six expander ports drop from 16 FPGA IO pins down to 14 FPGA IO pins with this chip
- DDR3 UDIMM 240 pin non-ECC 1.5V 1GB / 2GB / 4GB / 8GB DRAM
- 62.5MHz low jitter clock module
- Crystal oscillator, 62.5 MHz low jitter
- NXP LPC1111 50MHz Cortex M0 microcontroller
- Xilinx standard 14 pin JTAG header
- Two user controlled LEDs
- Two push buttons
- CR2032 battery slot

EXPANSION

Each of the six expansion connectors has the following features:

- 16 FPGA IO pins, usable as 8 differential pairs or as 16 single ended signals
- Support for one differential or two single ended global clock inputs
- 50 ohm single ended characteristic impedance
- 100 ohm differential characteristic impedance
- Edge connector maintains characteristic impedance across board to board boundary – never worry about impedance mismatch from 100 mil header posts again!
- Edge connector rated for operation up to 5Gbps per signal pair
- FPGA IO pins powered from main board 3.3V rail or from external user supply, selectable via jumper
- Compatible with Xilinx signaling standards:
  - LVCMOS
  - SSTL
  - LVDS
  - many others, see Xilinx UG381
- CN1, CN2 and CN3 connect to FPGA Bank 0 while CN6, CN7 and CN8 connect to FPGA Bank 2. Consult Xilinx UG381 regarding the capabilities of each IO bank
- One IO pin can be configured as VREF input
- 4 CPU IO pins, useful for low speed housekeeping tasks such as I^2C device interrogation



- Ground and VCCO power rails connected at multiple pins
- Unregulated 9V power also available at one pin
- Open drain Global Reset allows reset in and reset out

COMPATIBILITY

- Compatible with:
  - free Xilinx ISE WebPACK software
  - free Xilinx MicroBlaze MCS soft CPU
  - Xilinx ISE, EDK and SDK software
  - NXP LPCXpresso IDE for LPC1111

KIT CONTENTS

- FS6484 main board
- DDR3 UDIMM
- AC-DC power supply
- DRAM controller IP core DDR3 DIMM 604Mbps
- Reference design: MicroBlaze MCS + DRAM + UART + GPIO
- Manual and Schematic