

Low cost Xilinx Spartan 6LX development boards



Introduction

The FS604 and FS609 are compact, low cost development boards based on Xilinx Spartan 6LX FPGAs.

Features include 32MB DRAM, 512KB FLASH, a high quality clock source, two expansion connectors and a JTAG test access port for device configuration and debugging.

Applications

- ◆ Student lab demonstrator board
- ◆ 750MSPS oscilloscope capture buffer
- ◆ 375MSPS 16 bit DDS buffer
- ◆ Triple 1080i video frame buffers
- ◆ Robotic control

Physical

- ◆ Dimensions 76mm x 41mm x 16mm
- ◆ Weight
 - 23g FS60x main board
 - 29g with USB2V5A800 regulator
 - 124g packaged shipping weight
- ◆ Power consumption
 - 160mA typical from 2.46V rail and
 - 85mA typical from 1.23V rail

Key components

- ◆ Xilinx Spartan 6LX FPGA
 - XC6SLX4-3TQG144C (FS604)
 - XC6SLX9-2TQG144C (FS609)
- ◆ SDRAM 256Mb(16Mx16) DDR400
 - Samsung K4H561638
- ◆ SPI Flash configuration memory, 4Mb (2.7Mb FPGA 1.3Mb user)
- ◆ Crystal oscillator, 62.5 MHz low jitter
- ◆ Expansion edge connector, 64 way 1mm pitch 38 user IO (2.5V rail)
- ◆ Additional expansion connector, 16 way 0.1” pitch 8x2 receptacle 6 user IO (2.5V rail)
- ◆ Xilinx standard 14 pin JTAG header
- ◆ User controlled LED

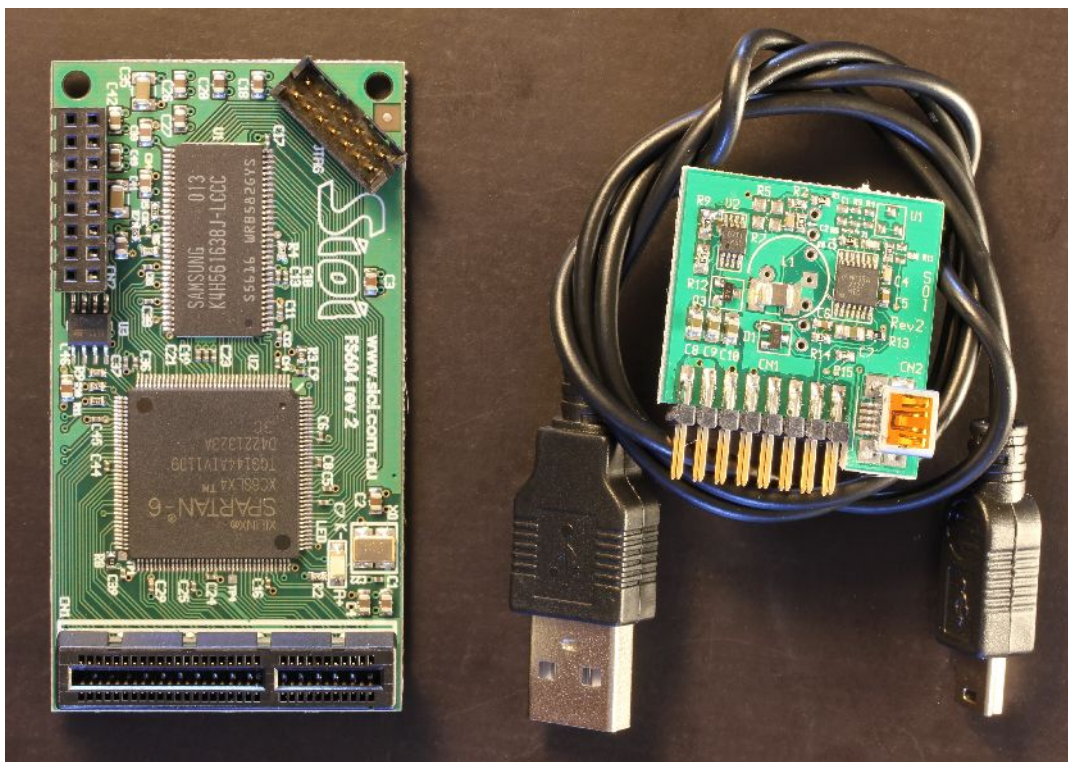
Customised versions

- ◆ Customised versions available upon request
- ◆ Industrial temperature range FPGA
- ◆ Other FPGA speed options
 - XC6SLX4-2TQG144
 - XC6SLX9-3TQG144
- ◆ DRAM 64 Mb / 128Mb / 256Mb / 512Mb / 1Gb
- ◆ DRAM DDR400 / DDR500 (64Mb or 128Mb only)
- ◆ Flash 4Mb / 8Mb / 16Mb / 32Mb / 64Mb
- ◆ 64 way expansion connector with daughter board parallel to the main board

Kit contents

- ◆ FS60x main board
- ◆ Power regulator USB2V5A800 (plug into a USB port to power unit)
- ◆ USB cable (power only)
- ◆ DRAM controller IP core DDR166
- ◆ Reference design: MicroBlaze + DRAM + UART + GPIO
- ◆ Manual and Schematic

Here's what you get:



Attaching the power regulator

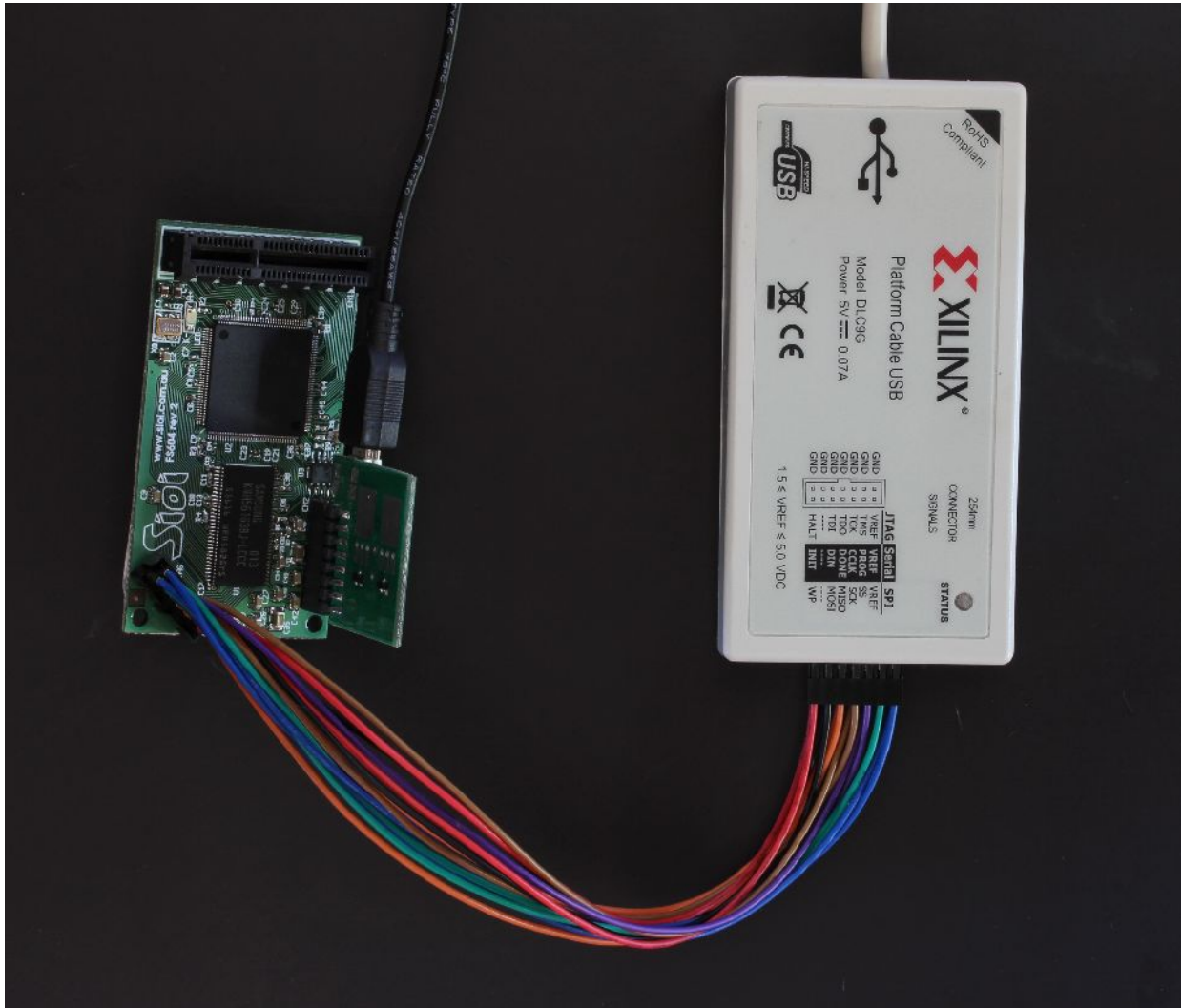
- ◆ Please attach the USB2V5A800 power adapter and USB cable like this:



- ◆ The USB2V5A800 and the FS60x board are keyed at pin location 11 to prevent incorrect insertion
- ◆ The correct order for connection is:
 1. Connect the USB2V5A800 to the FS60x motherboard
 2. Connect the USB cable to the USB2V5A800
 3. Connect the USB cable to a power source
- ◆ *If you apply power to the USB2V5A800 before connecting to the FS60x board then you might damage both boards. Please only apply power after these two boards are connected.*
- ◆ To reset the FPGA you need to disconnect the power and then reconnect it. The USB2V5A800 has built in circuitry to correctly reset the FPGA on power up.

Attaching a JTAG programmer

- ◆ To program the FPGA please connect a JTAG programmer like this:



- ◆ Use a JTAG cable that matches the Xilinx standard 14 pin 2mm pitch JTAG header
- ◆ The Xilinx brand USB or Parallel cables work well

Primary Expansion connector

The 64 way edge connector features 38 user IO pins which can be configured as 38 single ended IOs or as 19 differential IO pairs.

- ◆ Support for up to 4 differential or 8 single ended global clocks
- ◆ 50 ohm single ended characteristic impedance
- ◆ 100 ohm differential characteristic impedance
- ◆ Edge connector maintains characteristic impedance across board to board boundary
- ◆ Edge connector rated for operation up to 5Gbps per signal pair

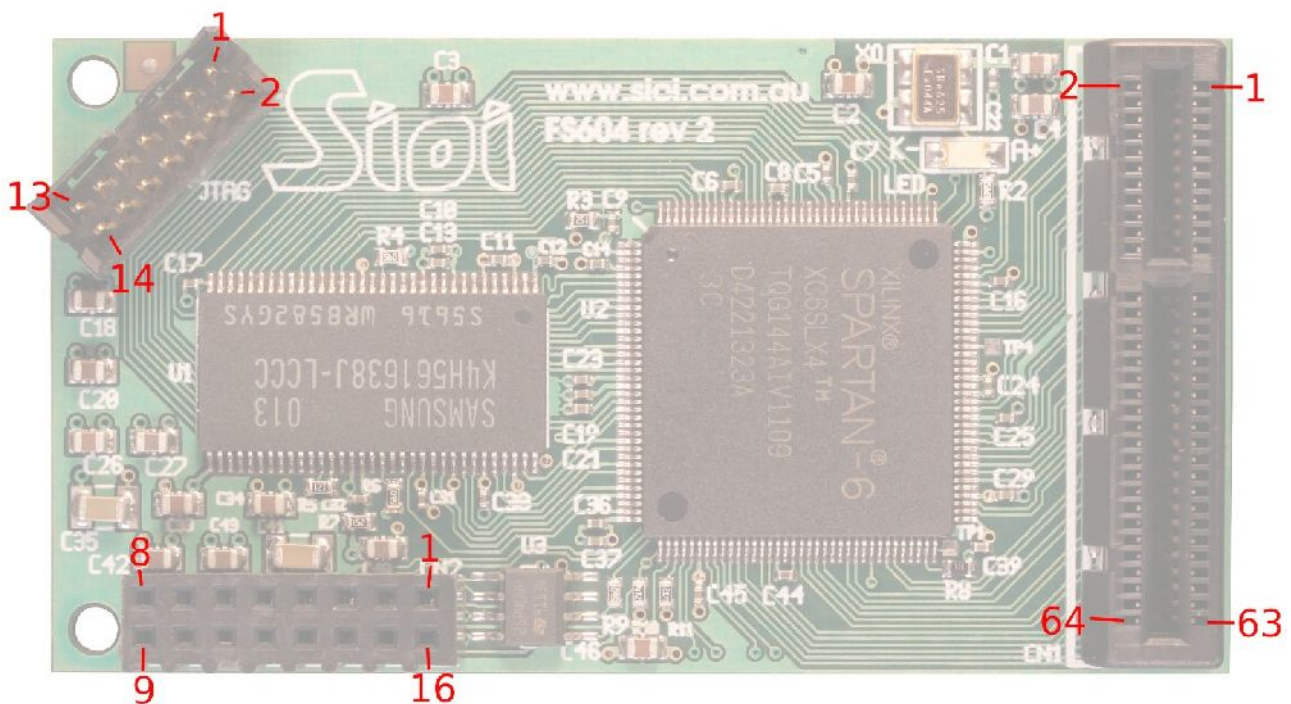
FPGA pin	IO bank	Corner	Pin name	Expansion pin	Notes
40	2	BL	IO_L64N_D9_2	CN64-35	
41	2	BL	IO_L64P_D8_2	CN64-37	
43	2	BL	IO_L62N_D6_2	CN64-43	
44	2	BL	IO_L62P_D5_2	CN64-45	
45	2	BL	IO_L49N_D4_2	CN64-51	
46	2	BL	IO_L49P_D3_2	CN64-53	
47	2	BL	IO_L48N_RDWR_B_VREF_2	CN64-61	optional despiker on secondary side
48	2	BL	IO_L48P_D7_2	CN64-59	
50	2	BL	IO_L31N_GCLK30_D15_2	CN64-62	GCLK capable
51	2	BL	IO_L31P_GCLK31_D14_2	CN64-60	GCLK capable
55	2	BR	IO_L30N_GCLK0_USERCCLK_2	CN64-58	GCLK capable
56	2	BR	IO_L30P_GCLK1_D13_2	CN64-56	GCLK capable
57	2	BR	IO_L14N_D12_2	CN64-54	
58	2	BR	IO_L14P_D11_2	CN64-52	
61	2	BR	IO_L12N_D2_MISO3_2	CN64-50	
62	2	BR	IO_L12P_D1_MISO2_2	CN64-48	
66	2	BR	IO_L2N_CMPMOSI_2	CN64-46	
67	2	BR	IO_L2P_CMPCLK_2	CN64-44	
74	1	RB	IO_L74N_DOUT_BUSY_1	CN64-42	
75	1	RB	IO_L74P_AWAKE_1	CN64-40	
78	1	RB	IO_L47N_1	CN64-38	
79	1	RB	IO_L47P_1	CN64-36	
80	1	RB	IO_L46N_1	CN64-34	
81	1	RB	IO_L46P_1	CN64-32	
82	1	RB	IO_L45N_1	CN64-30	
83	1	RB	IO_L45P_1	CN64-28	
84	1	RB	IO_L43N_GCLK4_1	CN64-26	GCLK capable
85	1	RB	IO_L43P_GCLK5_1	CN64-24	GCLK capable
87	1	RB	IO_L42N_GCLK6_TRDY1_1	CN64-20	GCLK capable
88	1	RB	IO_L42P_GCLK7_1	CN64-18	GCLK capable
97	1	RT	IO_L34N_1	CN64-16	
98	1	RT	IO_L34P_1	CN64-14	
99	1	RT	IO_L33N_1	CN64-12	
100	1	RT	IO_L33P_1	CN64-10	
101	1	RT	IO_L32N_1	CN64-8	
102	1	RT	IO_L32P_1	CN64-6	
104	1	RT	IO_L1N_VREF_1	CN64-4	optional despiker on secondary side
105	1	RT	IO_L1P_1	CN64-2	

- ◆ FPGA IO pins powered from 2.46V rail
- ◆ Compatible with Xilinx 2.5V VCCO signaling standards:
 - LVCMOS25
 - SSTL2
 - LVDS_25

- ◆ many others, see Xilinx UG381
- ◆ 18 of the IOs come from Bank 2 and 20 come from Bank 1. Consult Xilinx UG381 regarding the capabilities of each IO bank
- ◆ One IO pin can be configured as Bank 1 VREF input
- ◆ One IO pin can be configured as Bank 2 VREF input
- ◆ Ground, 1.23V and 2.46V power rails connected at multiple pins
- ◆ Unregulated 5V (USB) power also available at two pins
- ◆ Open drain Global Reset allows reset in and reset out
- ◆ The edge connector used is the same as that used for PCIE x4. It features a 1mm pitch and has 64 connections configured as a group of 22 and a group of 42 with a keying spacer between the two groups
- ◆ The edge connector used is FCI part 10018784-10201TLF or similar
- ◆ An expansion board template for gEDA PCB CAD package available as a free download from SIOI website

Connector orientation

The numbering orientation of the connectors is shown below:



Secondary expansion connector

The 16 way 8x2 100 mil pitch connector is primarily a power input but also includes connections to 6 FPGA IO pins, enough for low bandwidth peripherals. A connection to the open drain Global Reset signal is also provided.

FPGA pin	IO bank	Corner	Pin name	Expansion pin	Notes
38	2	BL	IO_L65N_CS0_B_2	FLASH CS pin, HDR16-16	terminate on HDR16 daughterboard
70	2	BR	IO_L1P_CCLK_2	FLASH-CLK, HDR16-2	
64	2	BR	IO_L3N_MOSI_CSI_B_MISO0_2	FLASH-DIN, HDR16-14	
65	2	BR	IO_L3P_D0_DIN_MISO_MISO1_2	FLASH-DOUT, HDR16-1	
92	1	RT	IO_L41N_GCLK8_1	HDR16-3	
93	1	RT	IO_L41P_GCLK9_IRDY1_1	HDR16-13	

The FLASH_CLK signal is terminated on the USB2V5A800 daughter board with a 50 ohm termination to the 1.23V rail.

Software Compatibility

- ◆ Compatible with:
 - free Xilinx ISE WebPACK software
 - Xilinx ISE, EDK and SDK software
 - Xilinx MicroBlaze soft CPU

FAQ

Q: Can I power the board from the 64 way expansion connector ?

A: Yes, you can power the board from the 64 way expansion connector. You need to supply 2.46V +/- 0.05V and 1.23V. Typical consumption is 160mA and 85mA, so design for at least twice that for safety. The 1.23V rail should be (50±1)% of the 2.46V rail as it is used for DDR termination and reference voltage. The TI TPS51100 is a suitable regulator for the 1.23V rail.

You do not need to supply 5V, the 5V rail simply runs from the 64 way connector to the 16 way connector in case you want to supply 5V from one connector and consume it at the other.

The FS60x has several bulk decoupling capacitors close to the 16 way connector. As you will be supplying power from the 64 way connector please supplement them by placing at least two 10uF ceramic decoupling caps for the 2.46V rail and at least two 10uF ceramic decoupling caps for the 1.23V rail on your daughter card, close to the edge connector.